BRIEF DESCRIPTION OF THE DRAWINGS

For a more complete understanding of the present invention, and the advantages thereof, reference is now made to the following descriptions taken in conjunction with the accompanying drawings, in which:

5   FIG. 1 is a block diagram of the architecture of a parallel pattern detection engine (PPDE) comprising N processing units (PUs) suitable for practicing embodiments of the present invention;

FIG. 2A-2D are block diagrams of four matching modes which may be programmed for each of the N PUs of FIG. 1;

10   FIG. 3 is a chart illustrating the various modes of scalability of the PPDE of FIG. 1;

FIG. 4 is a chart of performance results achievable by a PPDE integrated circuit employing 1500 PUs suitable for practicing embodiments of the present invention;

15   FIG. 5 is an overview block diagram of an individual PU in the PPDE of FIG. 1;

FIG. 6 is a detailed block diagram of an individual PU in the PPDE of FIG. 1;

FIG. 7 is another detailed block diagram of an individual PU in the PPDE of FIG. 1;

20   FIG. 8 is a circuit diagram of a specific implementation of a single PU in the PPDE of FIG. 1;

FIG. 9 is a flow diagram of method steps used in matching patterns suitable for practicing embodiments of the present invention;

FIG. 10 is the block diagram of a network processor (NP) suitable for 25   practicing embodiments of the present invention;

FIG. 11A-11G illustrate operation in various modes of pattern matching which may be used in embodiments of the present invention;

FIG. 12 is a block diagram of an intrusion detection system (IDS) according to embodiments of the present invention;